Small Times 2009 university report and rankings

by Pete Singer, editor-in-chief, and James Montgomery, managing editor, *Small Times*

In the past, universities and national labs were primarily focused on basic research. Once that research was concluded it was licensed to industrial companies, often through technology transfer offices. The problem with this model is that 80%-90% of the cost in commercializing a technology is in early development and manufacturing. This meant many technologies were never commercialized—or if they were, they took an inordinately long time (at least compared to today's standards).

A second model that evolved is the corporate integration model. In this case, researchers are given a specific target and are asked to align resources and manufacturing development research to support that end goal. Perhaps the most successful implementation of this model is the *International Technology Roadmap for Semiconductors* (*ITRS*, www.itrs.net). Launched in the early 1990s, it provided (and still does) a guideline for R&D for integrated circuit technology needs within a 15-year horizon. The first national technology roadmap efforts were sponsored by the Semiconductor Industry Association (SIA, www.sia-online.org) and supported by the Semiconductor Research Corp. (SRC, www.src.org/default.asp) which funded much of the university-based research. Examples of SRC-funded technologies include copper interconnects, strained silicon, high-*k* dielectrics and logic bricks.

Recognizing the potential of nanotechnology and the approaching limitations of CMOS scaling, the SRC created a new subsidiary in 2005 called the Nanoelectronics Research Corp., in order to develop and administer a university-based research program. Dubbed the Nanoelectronics Research Initiative (NRI, www.src.org/nri), its goal is "to demonstrate novel computing devices with critical dimensions below 10nm and to incorporate them into simple computer circuits that could enable the industry to extend Moore's Law improvements in electronics far beyond the limits of CMOS."

The NRI—which we'll investigate in more detail shortly—is a prime example of not only how nanotechnology is seen as the potential savior of an industry, but an indicator of how dramatically the landscape is changing for university research.

The changing landscape

While we believe the *Small Times* rankings stand on their own (*see page 3*), it became evident as we compiled the results that they did not fully capture the capabilities of various universities with regard to how successfully they (or maybe do not) network with other universities and research centers, particularly given the often dynamic nature of those relationships.

At Harvard University, for example, a professor is setting up a multi-university project for next-generation sensors. "Conceptually, it's a fantastic idea," said Daniel Behr, Harvard's director of business development, speaking at a recent forum near Boston with semiconductor industry executives. But practically, it would be a challenge to make happen, given concerns about who "owns" the IP or how it gets divvied up—and thus how each university monetizes its investments via licensing. (Eighty-five percent of equity from Harvard's licensing goes right back into the labs, Behr said, and 35% of all incoming money goes directly into inventors' pockets.)

IP is a battleground in corporate/university partnerships too, added Paul Farrar, VP for process development at IBM. If a business pays less, they should get less IP control, and vice-versa, he suggested. "Industry and academia need to get their heads around that." Protecting ideas is "a puzzling

Georgia Tech's Nanotechnology Research Center.

Nanotechnology university rankings

Successful universities are judged not only by the amount and quality of the basic research they do, but also on their capabilities to do mid- and short-terms research and how quickly they are able to help industry partners turn new technologies into commercial products. Of course, a host of other factors are also important including the number of students graduated, the number of academic papers published, IP licenses executed, patents awarded, the number of staff and research centers, annual budget, and partnerships with national and global institutions.

This year, as in past years, *Small Times* conducted a survey designed to evaluate which institutions are the "best of the best" in micro- and nanotechnology. The rankings are based on an in-depth questionnaire that gauges each university's capabilities and strengthss, compiled into two categories: research and commercialization. The rankings also include a "peer review" category that enables us to see who is tops in nano research not only according to the numbers gleaned from the surveys, but also in the opinions of those who are in the trenches of university nanotech work. This also allows us to include universities that did not respond (in detail or at all) to our call for participation.

"Top-10" lists of any kind are both popular and endlessly scrutinized. Ideally they are 100% data-driven, but inevitably subjectivity sneaks into the process. How did we decide what methods we used to combine, weigh, and compare sets of data in order to judge one school as "better" than another? How should we compare the numbers submitted by schools, vs. the opinions of those who rate their peers? Even in the wording of our survey questions, some inferred a predisposition toward certain types of nanotechnology (e.g., MEMS), vs. other aspects of important nanotechnology work.

In the end, we closely followed the structure and weightings of our past surveys, with minor modifications. We still believe combining certain criteria gives a better picture of overall themes—a school's facilities, spinoffs, patents awarded, and IP licenses, collectively paint a picture of its capabilities in commercializing its nanotechnology achievements, for example. But we also acknowledge our survey's limitations; it's not a perfect process, and we're always working to make it better.

For this year (the academic year ended July/August 2008), the race to be tops in terms of "Research" was tight—but in the end the #1 university according to our rankings is **Penn State**, drawing high marks across nearly every category, from facilities staff to funding (state/federal/industry/grants) to students and degrees conferred (BS/MS/PhD) to papers presented. Close behind is **Washington**, whose funding and BS degrees total more than a third higher than anyone else. Third-place **Maryland** and fourth-place **Cornell** are neck-and-neck in several categories, including papers presented and total micro/nanotech undergraduates. **North Carolina**, **SUNY/Albany**, **Pittsburgh**, **Purdue**, **Harvard**, and **NC State** round out the top 10.

In ranking schools' "Commercialization" capabilities, the runaway winner is the **U. of Albany**, which scored top marks in micro/nano patents, startups, and number of companies using their facility. With eight individual nanotech-focused facilities and an eye-popping 263 participating partners, the U. of Albany could arguably be considered a consortium—and in fact, semiconductor industry consortium SEMATECH has moved much of its leading-edge development work here in the past few years. A pack of companies fighting for position in the rest of the top-10 include **Cornell**, **NC State** (2nd to Albany in facility users), **Washington** (1st in IP licenses by a landslide), **Harvard**, **Pittsburgh**, **Louisiana Tech**, **Louisville**, **Central Florida**, and **Penn State**.

For our peer rankings, we essentially reverse-scored what people submitted as their top recommendations—e.g., a rank of "1" was assigned a value with the most weight, a "2" was one point below that, "3" a point below that, etc. We gave more weight to responders who submitted multiple rankings (at least 1 through 5), and used some common sense in calculating those who received disproportionately more or fewer votes. (One school's effort to "stuff the ballot box" for our online peer-rankings survey was extensive enough to pollute that entire effort—shame on them.)

Ultimately, there proved to be no single standout among peer-ranked universities, but several are among most people's favorites—and the lists looks a lot like it did in 2007. Kudos to **UC/Berkeley**, **MIT**, and **Michigan**, the clear 1-2-3 according to our survey respondents. **Stanford** and **Georgia Tech** are a fairly close 4th and 5th, followed by **Cornell**, **UCLA**, and **Carnegie Mellon**, and then a logjam including **Caltech**, **Columbia**, **Illinois**, **UC/San Diego**, and **Washington**. The Netherlands' **Delft U. of Technology** was one of 10 non-US institutions nominated by peers, but the only one to rank near the top according to our scoring. ST

COMMERCIALIZATION

1.	SUNY/Albany
2.	Cornell
3.	North Carolina State
4.	Washington
5.	Harvard
6.	Pittsburgh
7.	Louisiana Tech
8.	Louisville
9.	Central Florida
10.	Penn State

RESEARCH

1.	Penn State
2.	Washington
3.	Maryland
4.	Cornell
5.	North Carolina/Chapel Hill
6.	SUNY/Albany
7.	Pittsburgh
8.	Purdue
9.	Harvard
10.	North Carolina State

PEER NANO RESEARCH

1.	MIT
2.	Northwestern
3.	California/Berkeley
4.	Harvard
5.	Cornell
6.	Rice
7.	Illinois/Urbana-Champaign
8.	Stanford
9.	Massachusetts/Lowell
10.	Northeastern

PEER MICRO RESEARCH

1.	UC/Berkeley
2.	Michigan
3.	MIT
4.	Stanford
5.	Georgia Tech
6.	UCLA
7.	Cornell
8.	Delft (Netherlands)
9.	Maryland
10.	Illinois

PEER NANO COMMERCIALIZATION

1.	MIT
2.	Northwestern
3.	Cornell
4.	Harvard
5.	Stanford
6.	Rice
7.	UC Berkeley
8.	Caltech
9.	Illinois
10.	NC State

PEER MICRO COMMERCIALIZATION

1.	UC Berkeley
2.	MIT
3.	Michigan
4.	Stanford
5.	Georgia Tech
6.	Cornell
7.	UCLA
8.	Carnegie Mellon
9.	Caltech
10.	Columbia

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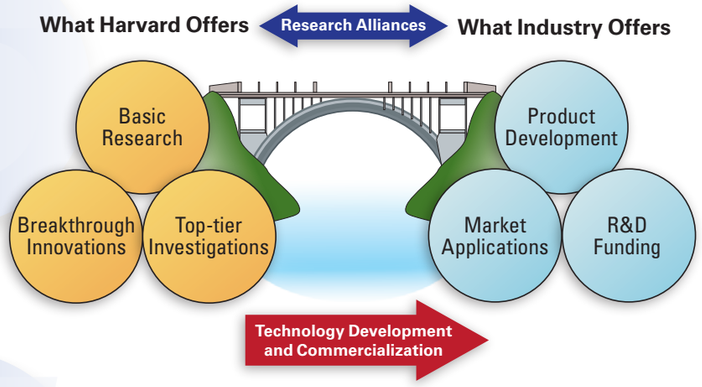
problem," acknowledged John Warlaumont, head of SEMATECH's site in Albany, NY, who oversees operations and strategy for the consortium's R&D programs. The semiconductor industry has been "very good at sharing its problems," he said, with everyone working on the fundamental R&D, and cross-licensing used to be much more common. Today the innovative spirit that sparked basic R&D is a big challenge, particularly for larger firms, because it essentially means embracing a likelihood of failure—and in today's business environment, noted Farrar, if companies aren't financially stable they can't (or won't) innovate.



Bridging the gap between academia and industry. (Source: Harvard)

This is where universities come in, claimed Paul McLaughlin, chairman/CEO of Rudolph Technologies. His own company's first product came out of Brown University; bigger companies didn't want it, but Rudolph got it because of the relationships it had already developed with key staff at the school.

This all speaks to a need to bridge the gulf between academia and industry perceived as a "Valley of Death," according to Harvard's Behr. Industry peers across the chasm and sees "mad scientists" cooking up innovations that are not "de-risked"—a euphemism for "more likely to fail or languish in a lab than be commercially useful. Academia, meanwhile, driven by pursuit of nobler intellectual aims, view relationships with industry as a "deal with the devil."

The key to bringing these two sides together, Behr explained, is to find common ground in broader collaboration in strategic areas, instead of the conventional one-off ad-hoc projects fitting a specific, short-term industry need. (He cited a 2007 initiative begun between Harvard and BASF, spanning five years and $15M-$20M.) Such collaboration reaches deeper into the university, including junior faculty, not just the well-known/connected researchers or the ones with IP, and involves as much "push" of idea generation from academia as "pull" from industry looking for solutions to problems. Both sides get what they want: researchers find motivation in available funding and exciting research opportunities, and companies get better access to breakthrough innovations.

Academia also needs to do better with the idea of "distributed innovation." This has been much more readily accepted and applied in the semiconductor industry, because customers are already far-flung (e.g. Asia) and consolidation among suppliers creates new and complex chains. Groups like the Semiconductor Research Corp. are making significant progress here, bringing together dozens of universities toward common research goals sponsored by industry.

The rise of focus centers

The primary goal of the Nanoelectronics Research Initiative (NRI), according to director Jeff Welser, is to "discover the next switch, a new mechanism for computing that goes beyond simply improving today's transistor." That means interacting with universities to "really make sure the pipeline is full of the research ideas we need, as well as the students that we need when they come out looking for jobs."

Jeff Welser, director, Nanoelectronics Research Initiative

About 25 years ago when the SRC was started, the focus was largely on funding small projects, one or two individual professors at universities across the US whose work was applicable to helping further the Moore's Law roadmap. "We tried to focus the research on things that were pre-competitive—things that we thought would help all of us but then we could take back to our labs, add our own secret sauce and make our products and still differentiate ourselves in the marketplace," Welser explains. "It was focused technology nodes maybe one or two nodes beyond what companies were doing in their internal labs."

Around the mid-'90s, however, the NRI realized there was also a need to look even further out—and universities has the best capability to do so. That realization resulted in the largest focus center research program to date. "It wasn't the first time we'd done centers, but it was certainly the largest scale we had ever done with multi-university centers and funding the whole center as a group," he said. This involved "substantial" financial support both from industry and DARPA, ~ $20 million from each.

"The way these centers were set up, there would be a lead university and a lead professor who would direct the center and it was largely up to them to come together with other universities," Welser said. "One of the things we'd require in the proposals for the centers is we wanted to see you pulling the best of the best from all sorts of universities around in the area that you are going to pursue, and set up your programs so that you're funding lots of different projects." NRI would assign a general area of focus but not a specific target; "if we're looking that far out, our guess from industry is not necessarily any better than the university guys' guess." In many cases the university researcher was given autonomy over decisions about program specifics, he said, because "they're more likely to go in some more adventuresome directions and take a few risks. They are often closer to the science and the base of materials work going on, so they might have some inkling of new areas before we would see them on the industry side."

The Microelectronics Advanced Research Corp. (MARCO), which manages the SRC's Focus Center Research Program, now has five focus centers under its umbrella: GSRC (Gigascale Systems Research Center), C2S2 (Center for Circuits and Systems Solutions), IFC (Interconnect Focus Center), MSD (Center for Materials, Structures, and Devices), and FENA (Functional Engineered Nano Architectonics). The collaborative effort involves 41 universities, 200 faculty, and 500 graduate students. All of the projects are multi-university, and because of this Welser said there has been a "real wealth" of different research ideas that have been developed. "Some of them that look really promising we wind up pulling directly into industry, if breakthroughs come through. Or sometimes some of those projects actually then wind up rolling into a bunch of other projects" in the SRC's main Global Research Collaboration (GRC) program, he said.

U. of Illinois' Micro and Nanotechnology Laboratory.

A multi-disciplinary approach

Nanotechnology extends well beyond semiconductor technology, into virtually every field imaginable—energy, agriculture, and biomedical, to name a few. Universities whose faculty is learned in multiple disciplines may have a leg up on those that don't. Another big factor—perhaps the biggest—is how well they are funded.

At the University of Illinois/Champaign-Urbana, nanotechnology requires "mega" dollars, notes Irfan Ahmad, associate director for the school's Center for Nanoscale Science and Technology. "You have to have large-scale investments in place to be able to conduct this sort of research." The pride of the U of I is its new Micro and Nanotechnology Laboratory. With 147,347 ft^2 of space, it is one of the nation's largest and most sophisticated university-based facilities for semiconductor, nanotechnology, and biotechnology research. It contains more than 8,000 ft^2 of class 100 and class 1000 cleanroom laboratories, a new 3,000 ft^2 laboratory complex specifically designed for bionanotechnology, and state-of-the-art, ultrahigh-speed optical and electrical device and circuit measurement equipment. Multidisciplinary research is carried out in four key areas: Micro- and nanoelectronics, nanophotonics and optoelectronics, nanomedicine and bionanotechnology, and MEMS/NEMS and integrated systems. The bionanosystems area focuses on utilizing the various technologies developed in materials, nanofabrication, devices, MEMS, and NEMS to study and solve biological issues.

Irfan Ahmad, associate director, Center for Nanoscale Science and Technology, U. of Illinois/Champaign-Urbana.

The U of I is one of 18 Nanoscale Science and Engineering Centers funded by the National Science Foundation (www.nsf.gov/about/budget/fy2009/pdf/37_fy2009.pdf). Others include Ohio State, University of California/Los Angeles, Rensselaer Polytechnic Institute, Columbia, Northeastern, University of New Hampshire, University of Massachusetts/Lowell, University of California/Berkeley, California Institute of Technology, Stanford, University of California/Merced, Northwestern, University of Pennsylvania, Arizona State University, University of California/Berkeley, Cornell, Rice, University of Massachusetts/Amherst, Harvard, and the University of Wisconsin/Madison (some centers include multiple universities).

"Nanotechnology is a multi-disciplinary field," notes Ahmad. The U of I not only has a very strong college of engineering but a very strong college of agriculture, liberal arts and sciences, a chemical school, and college of veterinary medicine. "All of this is under one umbrella which is quite unique. Some of the things we are currently pursuing are not only photonics and electronics but what we call nano-agriculture or also food and also cancer nano-medicine and the like."

This type of breadth in labs and facilities is just what the SRC is looking for, "because that kind of cross-talk that just happens by osmosis often times leads to very interesting ideas," says SRC's Welser. "The reason we tend to organize our centers to be multi-university is not necessarily just because we can't find all the right disciplines at a single university—in some cases you can—but rather to make sure that you're getting access to a wide breadth of ideas from different areas." Even support for those small projects hold promise because those 1-2 professors interact with others at their school and elsewhere, creating a "second-degree-of-separation access to some of the other work going on," he says. "The more of that you can pool with the limited amount of funds you have available, the better off you are in collecting that information." SUNY-Albany has many researchers exploring in energy and semiconductors, as well as bio, all in the same new facilities. "That's a great example of where we expect to see a lot of cross-talk and we hope to benefit from that," Welser said. "But if there's another school that has a smaller facility that's really only focused on semiconductors, that's fine too—if they have some good materials and good work going on and a professor there, we'd still love to have that person as part of our multi-university center and take advantage of getting him interacting with other universities."

SUNY-Albany's "cross-talk" is by design. The college emphasizes "a cross-disciplinary skill set" encompassing nano-bio systems, optoelectronics, nanoeconomics, and a range of semiconductor processes including 3D integration and lithography. "We like to say we're developing a Nano-Mall with some anchor tenants and boutique companies," explains Mike Fancher, VP for business development and economic outreach at the U. of Albany's College of Nanoscale Science and Engineering, and associate professor of nanoeconomics. Certainly the Albany Nanotech center is one of the largest and best-funded in the world, with 150 industry partners, $4.2 billion in funding, and staff (including partners) of about 2800 people. Just one example of the cross-disciplinary activities at Albany Nanotech: a symposium last year that attracted a group of accomplished experts in various fields of nanotechnology, biotechnology, medicine, and commercialization that came together to learn about the convergence of nanotechnology and biotechnology, and explored the cross-field fertilization opportunities.

One of the projects that University of Illinois's Ahmad is involved with also exemplifies the diversity of nanotechnology research—the goal is to detect soybean rust spores using wireless biosensors based on bio-photonic nanocrystal sensors produced by the school's engineering department. "Soybean rust spore is a big concern to the USDA and others; it can decimate the soybean crop," he explains. The group's work aims to "detect those spores and then make guidelines to help assist with the eradication of it." Meanwhile, Illinois researchers are working on sensors to detect food pathogens, he noted.

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Another U of I project is focused on nanomedicine for cancer research, in collaboration with international partners like the University of Karachi in Pakistan (www.uok.edu.pk/) which provides plant extracts. "We use those on biophotonic sensors here to test which of the extracts cause cancer cell pathos or death and also if any of these can be utilized for other infection diseases like malaria, tuberculosis and the like," Ahmad said. "There are 24-25 faculty members involved in cancer nanomedicine both in nanofabrication and cancer theragnostics—both therapy and diagnostics together." What helps with this work is that the U of I is also home to the National Center for Supercomputing Applications. "We are able to do some high-performance computing using modeling and simulation tools that look at ion channels for each single cell and the interaction with drug," said Ahmad.

NanoTech complex at the U. of Albany's College of Nanoscale Science & Engineering.

Another brand-new nanotech center is the Marcus nanotechnology research center at Georgia Tech (named after Bernie Marcus, one of the founders of Atlanta-based Home Depot). James Meindl, director of the Joseph M. Petit Microelectronics Research Center and the founding director of the Nanotechnology Research Center at Georgia Tech, explains that one of the facility's unusual features is that only about two-thirds of its 30,000 ft^2 cleanroom space will be inorganic (conventional semiconductor cleanroom space). The rest will be used for organic or biological research in nanotechnology. "There will be pass-throughs between these two kinds of laboratories," he promises.

The school's dedicated Petit nanotechnology building (with 8500 ft^2 of cleanroom space), which has been functioning for over a dozen years, will remain operational, Meindl said. "Last year [ending Feb. 28] we supported with our tools and staff and process inventory over 550 users who came to us for access and support and used nanotechnology to create new products. Of the 550 users, about 220 of them were from outside of Georgia Tech. Of those outside of Georgia Tech, about 150-160 were from other universities, and the remainder were from companies that wanted to use our facilities." Among its roster of customers: Intel and SanDisk, as well as Kimberly Clark, the maker of Kleenex.

The center has also supported strongly its startups. Cardio MEMS, capitalized at over $25 million with new venture funds, has developed "several hundred prototypes of a totally implantable, wireless pressure sensor which is implanted within the aorta of a person who has had an aneurism that's been repaired," said Meindl. "The pressure sensor is inserted in the aorta in order for a physician to be able to interrogate the pressure in the aorta wirelessly for years and years."

Another startup, Suniva, is a solar panel manufacturer, initiated about 15 months ago in Atlanta with about $50 million in capitalization. They presently manufacture about 32MW of solar panels, and have been a big user of the nanotechnology research capabilities of the Petit microelectronics cleanroom.

Georgia Tech's goal with its Petit facility and new Marcus center is "to be the hub of nanotechnology research in the Southeast—and we want to be unsurpassed nationally," Meindl said. "The way we're growing and serving users and the way we're building the space is promising." The reason, he says, is that Georgia Tech's school of engineering graduates more engineers than any other US university. "That's why we have such a growing number of users. With this new facility added to our capability, we want to become unsurpassed in our nanotechnology research activity. That's a big goal but that's what we have."

The funding challenge

All the top universities are in a race to find funding from all possible sources, including the federal, state, and local governments and from industry partners. It is this funding that enables them to do the basic research, build and equip state-of-the-art facilities that enable commercialization, as well as host symposiums, conduct outreach programs, and do all the other things that well-run universities do.

"We get funding from NIST primarily for our centers from the federal side," notes SRC's Welser, but a lot of the NRI center funding also comes from state and local governments. "This is a new partnership now, where you've got industry, the universities and state and local governments supporting the centers," he says. "The reasons the states are doing it are for the same reasons we have the federal partners—they know whoever finds 'the next switch' even at the state level might actually benefit more quickly, sort of the way that Silicon Valley grew up around the transistor." If, for example, the key breakthrough in a nanoelectronics switch happens at the INDEX center in Albany, NY, "they would have a good head-start there on actually building up their local economies and local businesses around that."

The newest NRI center, the Midwest Institute for Nanoelectronics Discovery (MIND) headquartered at Notre Dame University, received $1 million from city of South Bend to help them get started. "They saw this as something important not just at the state level but in their local community," Welser noted. "Nanoelectronics and nanotechnology is seen as a good place to put some money even at the basic research level with the hope that it's going to result in new ideas that will come out as future products and future business for their area."

Wolfgang Porod, director of the Midwest Institute for Nanoelectronics Discovery (MIND) at Notre Dame.

The MIND research team includes Purdue University, Penn State, Illinois, Michigan, Florida State's National Magnet Lab, and the University of Texas at Dallas, with research collaborations linking the National Institute of Standards and Technology, Argonne National Laboratory, and the National High Magnetic Field Laboratory. MIND research is organized around two concepts: energy-efficient devices and energy-efficient systems. The energy-efficient theme includes development of several types of devices:

- Tunnel transistors with low voltage and low subthreshold-swing,
- Graphene transistors based on spin, tunneling, and thermal rectification,
- Quantum transport modeling tools for MIND devices,
- Engineering of energy dissipation in nonequilibrium devices, and
- Magnetic quantum-dot cellular automata.

"A significant package was put together with matching by the university, matching by the state on the order of $10 million, and the city of South Bend also contributed $1 million, with an additional $60 million in terms of funds that are available if companies are interested in moving to this area," notes Wolfgang Porod, director of the MIND center. This is related to an Innovation Park, a technology park under construction adjacent to the Notre Dame campus started in partnership with the university and the city and state, which is seeking foundation tenants. An additional effort is being made to turn an area where Studebaker cars were once made—the so-called Studebaker Corridor—into a technology park as well, called Ignition Park. "There's also some land a couple of miles from campus that is being provided by the city for economic development to the tune of $50 million or so," Porod added.

The willingness to fund university research at the state and local level also reflects the changing nature of R&D. "Time has become a major focus for the industry," said Albany's Fancher. "They are trying to compress that timeframe from moving from fundamental research into production. The costs have gotten so high that it's really required a 'triple helix' of industry, university, and government participating in the model in very real ways." The state of New York, for example, has committed $800-900 million to date to efforts in Albany, while the industry committed the other $3.5 billion, he said.

U of I's Ahmad agrees. "One of the key things that's happening right now is there's a paradigm shift in terms of not only conducting the basic research but how you translate it to the commercial scale." Over the last few years, funding from sources such as the NIH has been "pretty much focused on translational research." Universities need to demonstrate that they are nimble enough, he advised, and provide evidence that they are taking it to the next level. The catch is, "how do you gauge that?"

The next switch

The priorities universities place on the funding they do receive may be changing, too. "In terms of how universities are being utilized, one of the things we've gotten much better at as an industry is realizing that you don't necessarily need to control every penny what is the deliverable you expect to see from that at the end of the year," Welser explains. "That works very well for research that's close enough, but for this further out work, you're better off to let the greater minds of the universities work on something and think it through a bit, and just be more mentors and liaisons to that work."

In the NRI program, industry liaisons from companies go and actually work on campus at the centers on full-time assignments. "That's part of the dues that the NRI member companies pay—they get part of that reimbursed by having a full-time assignee working at one of the centers," he said. "They are really right there trying to do research with the university guys—they aren't project managers sitting there trying to figure out if you're reaching your milestones. That way, when you get a physicist working on something and he's got some great idea, you've got somebody there next to him that can say okay, let me understand

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what the on-off ratio is on this or what it could be, or what kind of temperatures it would actually operate at—all sorts of questions an engineer would ask early on." For example, much of the semiconductor nanoelectronics research takes place at very low temperatures, which would be impractical in real-world applications. "If there's an interesting science effect at 4°K and it will always be at 4°K, then it's probably not something we want to spend a lot of time with at NRI," Welser explained. "On the other hand, it might be a really interesting science effect at 4°K and you might continue to do a lot of science work at it at low temperature, but at the same time work out what are the limits of that temperature. Are there ways to get it to higher temperature? We've definitely seen examples of that already whereby asking that question early on you find out pretty rapidly that this is something that can operate at room temperature."

Mike Fancher, VP of business development and economic outreach, U. of Albany's College of Nanoscale Science and Engineering.

Some physicists may cringe at how much influence the semiconductor industry has on the direction of nanoscience. Albany's Fancher points out, though, the *International Technology Roadmap for Semiconductors* has been a driving factor in enabling nanotechnology convergence. "Nanotechnology entered the roadmap in the 21st century, primarily focusing on high-performance computing. But when you think about this, you've got to go back and redo your research. You have a four-factorial increase in the number of roads to go down as you introduce, let's say, quantum dots or spintronics or moletronics. How do you pattern for spintronics? What kind of new materials do you need for integration?"

What is truly the most exciting is the notion of pro-active computing and convergence, Fancher says. "A lot of that is coming out of the research that's being done by the semiconductor industry to move a signal around on a chip. That know-how can now be applied to energy challenges and bioelectronics and a whole host of other applications."

That need for a new switch has required a change in the types of professors involved in the research. "We branched out in terms of the kinds of professors and places we were working with. MARCO is largely electrical engineers and materials science engineers—people who are on the engineering side of things," Welser said. Many professors in the NRI program are physicists and chemists, he points out. "Because a lot of the work that we're doing is really at the forefront of scientific knowledge on some of these materials, you actually need the science guys there. And the hope is that by pulling the science guys and the engineering guys together into these centers, you get a conversation going and hopefully advance science ideas more quickly into potentially usable devices or usable technology."

One of the most promising candidate for the next switch was pioneered at Notre Dame, according to Porod. "There's quite a bit of work going on across the NRI to look at spin-based state variables," he said, exploring how to extend magnetism beyond storing data to doing logic, he said. "For information processing we for the most part use charge, but there are some prospects of also basing information processing on magnetic phenomenon." Notre Dame is working on a more general scheme called quantum dot cellular automata (QCA), though it's not really quantum dots, he explains, but a different way to represent information by the arrangement of charges, rather than their flow. "A scheme like that is inherent in lower power and it also works for magnetic implementation. Instead of having arrangements of charges, we can also work with arrangements of magnetization—essentially flipping magnetizations to manipulate information," Porod said. "We've pioneered QCA for quite some time—and I think it helped us win this SRC center."

Conclusion

Universities have evolved over the years from places of higher learning and basic research to well-funded powerhouses that are hubs of industry development and commercialization. They are not only home to the country's most promising technology incubators, but true centers of education, often reaching out to the local community's grade school and high schools to share the excitement and opportunities of nanotechnology, science, and engineering.

In this report, we have provided an outlook from a select group of exemplary universities, demonstrating the breadth or research efforts, the evolving nature of R&D, and the importance of a multi-disciplinary, multi-university approach. We also offer a set of rankings based on our annual survey. Our focus was primarily on nanoelectronics research, which naturally had origins in the semiconductor industry and has since grown to include biomedical, energy, and many other applications.

Of course, there are many universities we did not cover, and we encourage readers to look for other reports on university research. One of the most comprehensive is that offered by the Center for Measuring University Performance. Their most recent report, *The Top American Research Universities* (mup.asu.edu/research2008.pdf), notes that "The process of ranking universities continues as a popular and controversial effort on a national and international scale, and the proliferation of rankings of all types has sometimes improved our understanding of research university competition and at other times provided considerable entertainment." Hopefully our report provided more of the former than the latter. In any case, the authors salute the hardworking men and women at all universities around world, and wish them the best of luck in what is undeniably the fun and fantastic world of nanotechnology. ST

Industrial Applications Demanding Low and High Resolution Features Realized by Soft UV-NIL and Hot Embossing

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ABSTRACT

There are several applications either currently in production or in late stage R&D, for UV-based Nanoimprint Lithography (UV-NIL) and Hot Embossing (HE) that require a full-field imprint technology in order to make these processes either feasible or cost-effective. These applications cover a wide range of features sizes from the millimeter range down to sub-100 nm. Because of the total thickness variation (TTV) associated with the imprinted substrates, full-field imprinting requires fabrication of a "soft" or "working" stamp from a "hard" stamp usually made from materials such as nickel, quartz or silicon. Several materials and processes have previously been identified that allow for full-field imprinting, however, these materials all have drawbacks associated with them that hinder their movement into High Volume Manufacturing (HVM) environments. EV Group Inc (EVG) has, in cooperation with our NILCOM™ partners, identified a novel set of polymeric materials and stamp fabrication processes that allow for full-field imprinting solutions suitable for these HVM environments. These materials have proven effective for imprinting at both millimeter feature sizes all the way down to 50 nm – full field. These materials, and the processes associated with their fabrication into working/soft stamps, should allow for a superior cost-of-ownership benefit and facilitate the movement of imprint lithography into industrial applications.

Key Words: Nanoimprint, Hot Embossing, UV-NIL, soft UV-NIL, HE, sub-100 nm features, soft stamps, working stamps, de-embossing, large area imprint, full-field imprint.

INTRODUCTION

As imprint lithography applications move into manufacturing environments, there are several applications that are moving towards full-field imprint due to the throughput and process advantages afforded by this method over traditional step and repeat imprinting. The move to full-field imprinting is usually a necessary step for cost-effective manufacturing whether the applications are for fine resolution (e.g. photonic crystals or patterned media) or larger feature sizes (e.g. micro-lens for CMOS image sensors). Traditionally, achieving fine feature resolution (< 100 nm) with UV-NIL has been accomplished using hard, quartz stamps [1]. The non-planarity that is associated with standard substrates limits the active area of these stamps to ~ 25 mm x 25mm - requiring a step and repeat approach to imprinting the entire substrate surface [2]. While the step and repeat process is necessary for certain applications requiring fine alignment, it is time consuming, requires specialized equipment sets to accomplish and can encounter

stitching issues for certain devices. Fine features sizes of less than 100 nm can also be realized with hot embossing into spun-on polymer resists. The challenges here include, not only the TTV of the imprinted substrate, but also the de-embossing of the stamp after the resist has cooled to below Tg [3]. Additionally, there are several structuring processes at larger feature sizes, up to the millimeter range, that use imprint lithography to achieve a desired device form factor. All of these applications can take advantage of the higher throughput and process benefits (e.g. lack of stitching requirements) afforded by a full-field imprint.

Full-field imprinting is typically realized by the fabrication of a "working" or "soft" stamp using a hard stamp as the template also known as the "master". This hard master can be of various materials such as nickel, quartz or silicon. The patterning of the master for fine resolution is usually performed via e-beam lithography. For larger feature sizes, master fabrication can employ other methods such as standard optical lithography or diamond turning. This working stamp can then be used in a full-field imprinting process commonly termed as "soft UV-NIL".

In order to provide an effective, full-field imprint the working stamp must have the ability to conform to the TTV of the imprinted substrate while maintaining the fidelity of the desired features defined by the master stamp and have a low surface energy to facilitate the de-embossing process. Typically, working stamps fall into two groups: soft, polymeric stamps and hard, flexible stamps. Both methods face issues in their fabrication and during the imprint process that can make their transition to high volume manufacturing environments challenging. For instance, soft working stamps are typically made from Polydimethylsiloxane (PDMS) because this material provides a low surface energy and good conformal qualities. But, PDMS requires a long, thermal cure under pressure which is very time consuming and can take several hours [4]. Therefore, this process is not conducive to high throughput applications. The material has other issues like swelling when in contact with organic solvents. It also experiences shrinking during the curing process which requires biasing of the features on the master. Also, since PDMS easily conforms to substrate TTV, it presents challenges when attempting to imprint fine feature sizes. Multi-layer PDMS stamps have been fabricated that allow for sub-100 nm feature sizes, however, the compliance of the material still presents challenges for maintaining good pattern fidelity during imprint [5].

Thus, in order to achieve high pattern fidelity in the transfer process, hard and flexible working stamps can be used. These stamps are typically made of thinned, and thus flexible, glass with the master stamp pattern transferred into the imprinting surface through an imprint and etch process [6]. While this method allows for fine feature sizes (sub-50 nm) to be transferred to an imprint resist with good fidelity, these stamps have several issues that make them undesirable for manufacturing applications. Firstly, their fabrication typically requires an imprinting and etch step into the hard substrate – which is costly and time consuming. Secondly, an anti-stiction layer needs to be applied and monitored during processing to assure proper de-embossing which adds additional equipment and process steps. Finally, the thickness of these substrates makes them delicate and difficult to handle.

In this paper, we, in collaboration with our NILCom™ partners, will show results from engineered, polymeric "working stamps" fabricated with a novel set of materials and with demonstrated resolution down to 50 nm over an area of up to two inches. These materials are either currently commercially available or in pilot production stage. In addition to the benefit of high resolution, these materials offer several other processing and cost-of-ownership benefits when compared with competing solutions - including faster and simpler fabrication. The working stamp can be made directly from the master. There is no need for imprinting, etching or thermal cure. Also, one can fabricate sub-masters from the original working stamp using the same class of materials - providing greater flexibility for the master fabrication. The working stamp (and sub-masters) can be fabricated very quickly (a matter of minutes) using only a standard mask aligner as the materials only require UV curing. The stamps have shown the ability to handle multiple imprints per stamp (> 100 imprints). Additionally the materials, like PDMS, have inherently low-surface energies so an anti-stiction coating does not need to be applied or monitored during imprint processing. These materials have great processing flexibility. For example, they can be used to process large features (e.g. millimeter size micro-lenses). And finally, to demonstrate the material's process flexibility and low surface energy, these materials have also been used for hot embossing into spun-on resists with resolution down to 50 nm feature sizes.

EQUIPMENT

The set of materials that are being demonstrated as working stamps for this paper are UV curable materials and thus can be fabricated directly from the master stamp on the same mask aligners that are used for the soft UV-NIL process. The processes discussed in the Results section of this report have been demonstrated on both the EVG620 and the EVG IQ Aligner mask alignment systems (Fig. 1, 2). The EVG620 can handle substrate and stamp sizes from pieces up to 150 mm. The IQ Aligner is designed for substrate sizes from 100 mm to 300 mm. Both systems are capable of semi-automated and fully-automated configurations for soft UV-NIL applications.

Fig. 1: Semi-automated EVG620 soft UV-NIL system for R&D and pilot line production

Fig. 2: Fully automated IQ aligner for soft UV-NIL industrial applications

In addition to the soft UV-NIL processes, these materials have also been tested for hot embossing applications on the EVG750 (Fig. 3). The EVG750 is the first commercially available, fully-automated hot embossing system. It can provide high force – up to 600kN – with 120 kN being the standard configuration. The tool also provides top and bottom side rapid heating capability up to 250 ºC. Rapid top and bottom side cooling is also part of the standard configuration.

Fig. 3: Fully-automated EVG750 Hot Embossing System for industrial applications

STAMP FABRICATION

The working stamp fabrication takes place on a standard mask aligner. The patterned master is simply placed on the bottom chuck in the aligner and a blank mask backplane is loaded into the mask holder. The uncured stamp material is then puddle dispensed on the master stamp. The glass backplane and the master stamp are then brought into contact and a low contact force of roughly 100N is applied. Depending on how the tooling for the mask aligner is configured, a low vacuum (~ 5 to 10 mbar) can also be applied but is typically not necessary. Once the force has been applied and the resist has spread to the desired coverage of the stamp-backplane interface, the material is flood exposed with broadband UV light. The material is cured within approximately one minute and the fabricated working stamp and can then either be separated from the master stamp automatically in the mask aligner or manually de-embossed outside the mask aligner.

Another useful aspect of these working stamp materials is that, with certain facile process adjustments, one can fabricate another working stamp from a working stamp that was initially fabricated off the master stamp while maintaining pattern fidelity. There are several phrases that have entered into the technical lexicon that describe the “lineage” for this working stamp process flow. Thus, the working stamp fabricated from the master stamp is also called either the “sub-master” or the “daughter” stamp. And, if a working stamp is fabricated from this “sub-master/daughter” stamp it is then called a “sub-sub-master” or “granddaughter” stamp. The ability to fabricate a granddaughter stamp from a daughter stamp with the same UV curable material set affords the user great flexibility when fabricating the hard master stamp. In Fig. 4, it is apparent that one can use this

technique to imprint positive features into resist by using a master with negative features – which is typically much easier to fabricate than a master with positive features. This can be accomplished with these working stamps while still maintaining excellent pattern fidelity (see the RESULTS section).

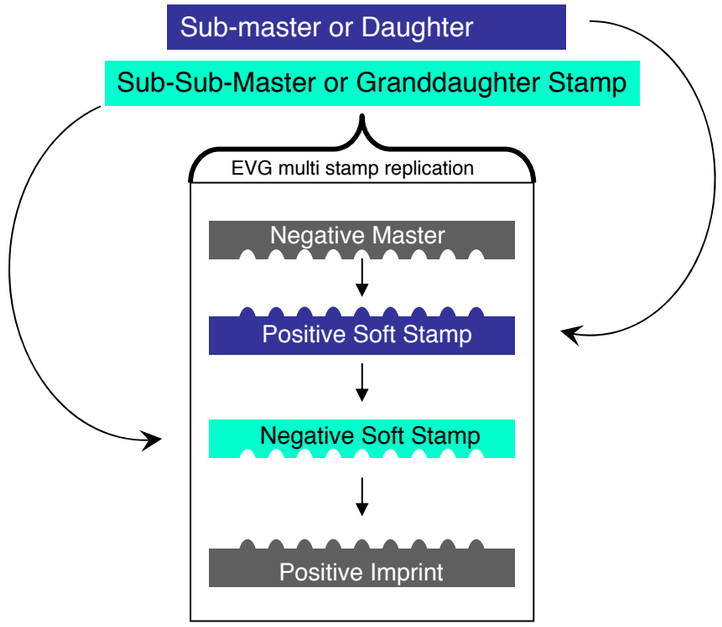

Figure 4: Replication process for a “lineage” of working stamps from a hard master

RESULTS

The soft UV-NIL process flow described above in Fig. 4 was tested on an EVG mask aligner using a standard silicon *NIL Technology* master, a commercially available resist from *micro resist technology* and the UV curable working stamp polymers. A daughter stamp was fabricated on the EVG620 using the master. Then a granddaughter stamp was fabricated from the daughter stamp. The total time for completion of these processes was less than 10 minutes. The granddaughter stamp was then imprinted into the resist using the same EVG620. The resulting imprints were then analyzed on an atomic force microscope (AFM) across a total of 75 measurements. The AFM results showed that the granddaughter stamp material was able to imprint features from the hard master stamp into resist with resolution down to 50 nm and with pattern fidelity of approximately 5%. The granddaughter stamp and the imprinted silicon substrate were successfully de-embossed in the aligner in an automated fashion.

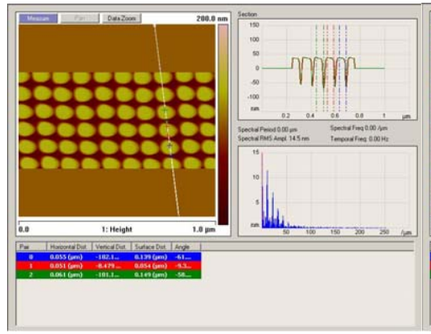

Figure 5: AFM image of the silicon master with dots (50 nm in diameter and 98 nm in height) used for working stamp fabrication

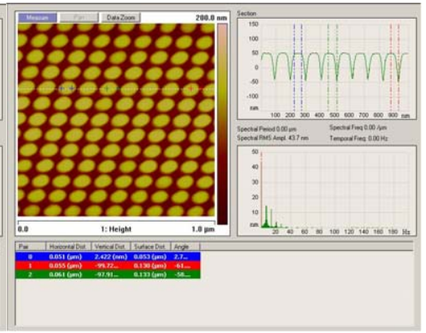

Figure 6: AFM image of the corresponding imprint on a silicon substrate by using a granddaughter working stamp from the silicon master shown in Figure 5

Additionally, a hot embossing test was performed on the EVG750. The purposes of this test were to both understand how the working stamp materials perform under hot embossing conditions as well as to gain an empirical understanding of the limits of the de-embossing capability of the working stamp materials. The same *NIL Technology* stamp was used once again to fabricate a working stamp by the previously described method. The backplane with the patterned working stamp material was then loaded into the EVG750 and an imprint was performed at 150 ºC into a commercially available *micro resist technology* resist that had been spun onto a silicon wafer. The resulting imprint (Fig. 7) allowed for facile, automated de-embossing of the stamp post-imprint without any residuals on the stamp or the imprinted wafer. Typically, automated de-embossing of such fine features into a spun-on HE resist layer presents significant challenges due to the high surface area in contact between resist and stamp.

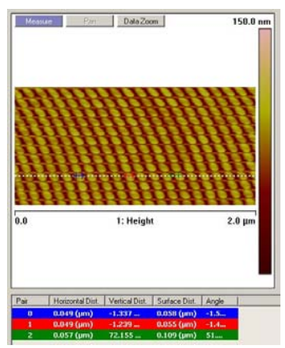

Figure 7: AFM image of imprinted features with 50 nm resolution

As mentioned above, these working stamp materials can imprint both small and large feature sizes. Below (Fig. 8 and Fig. 9) are images of a 200 mm glass wafer imprinted with micro-lenses for wafer level CMOS camera fabrication. Automated de-embossing at 200 mm is a proven process for these materials and 300 mm automated de-embossing has been demonstrated in the IQ Aligner as well. This is an application already in a

manufacturing environment where the material of choice for the working stamp is typically PDMS. The ability to use these alternative materials will allow for faster fabrication of the working stamp as well as other processing advantages mentioned in the Introduction.

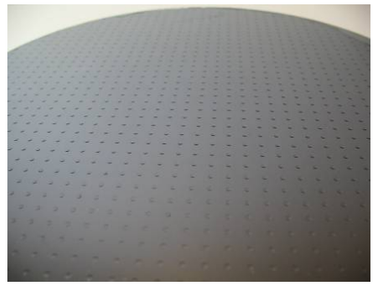

Figure 8: Image of an array of micro-lenses (diameter of lenses: 1 mm, height of lenses: 500 μm) imprinted with working stamp on 200 mm glass wafers

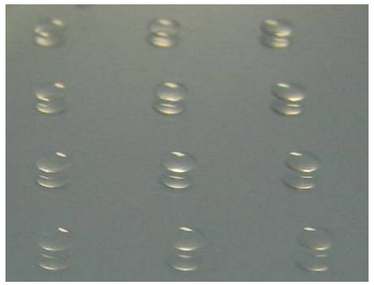

Figure 9: Image of an array of micro-lenses imprinted with working stamp on 200 mm glass wafers (close-up from figure H)

CONCLUSIONS

Full-field soft UV-NIL and hot embossing was successfully demonstrated for large and fine feature resolution using a novel set of polymeric materials for the working stamps. These materials are either already commercially available or sit in the pilot production stage. They offer several advantages over current working stamp technologies for industrial applications. These advantages include: inherently low surface energy (no anti-stiction layer needed); fast fabrication directly from the master stamp – no imprinting or etching required; fabrication capability on the same platform employed for the UV-NIL process; the ability to make granddaughter stamps and excellent imprinted pattern fidelity.

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